**4-Bit Binary Counter**

a 4-bit binary counter circuit that increments (or decrements) on each clock pulse.

Components required to build

1. 4-bit register
2. ALU
3. Reset to zero option

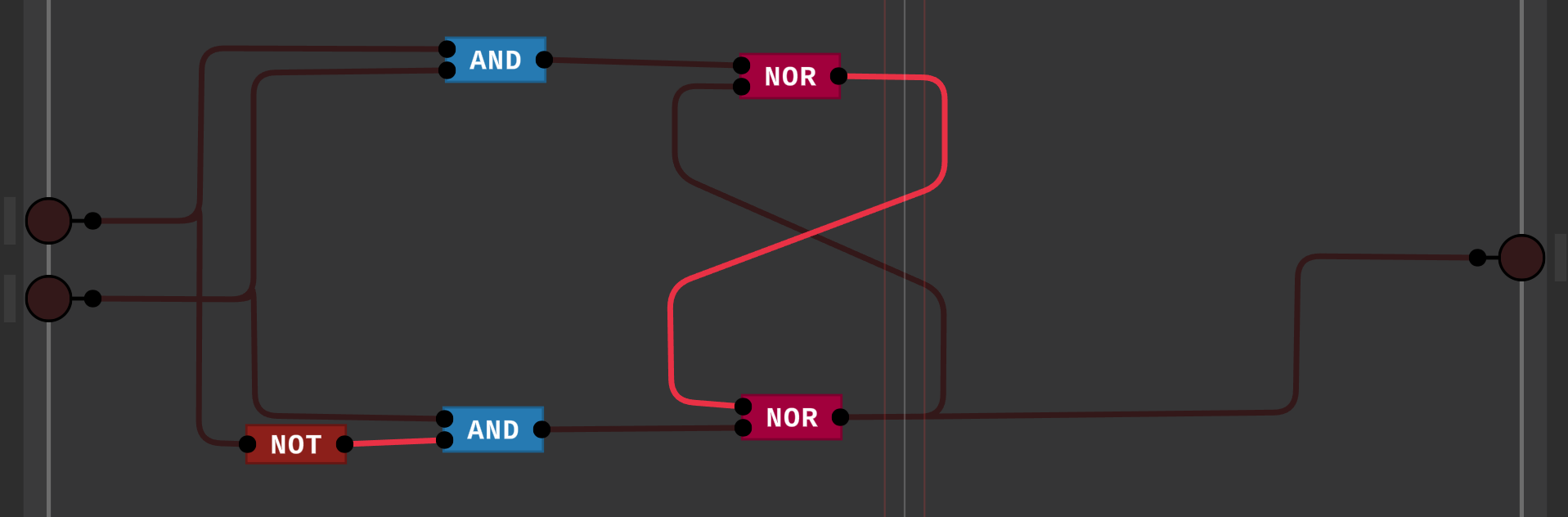
I)4-bit register

i)D Latch:

A **D latch** is a type of logic circuit that holds and stores a single bit of data. It has two primary inputs:

1. **D (Data)** - Input signal to be stored.
2. **E (Enable)** - Controls when the latch updates its output.

Working :D Latch stores the data that is present in the data pin to the output pin when the store pin goes from 0 (low) to 1(high)

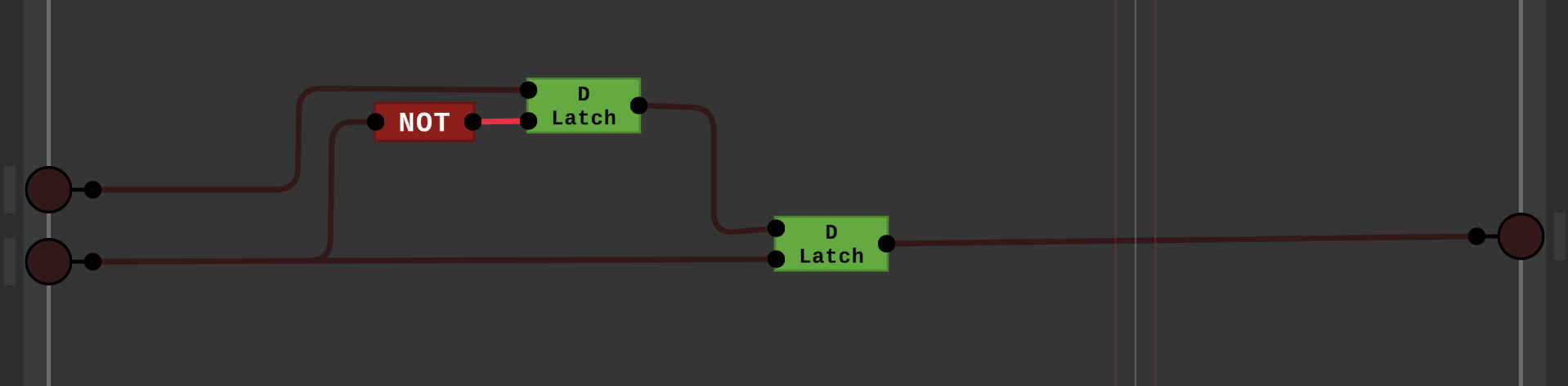


If E is offed, the data pin will not affect the output pin, if E is on any data present in the data pin will get stored in the output pin.

ii)D Flip Flop:

A **D flip-flop** is a sequential logic circuit that stores one bit of data and operates on clock edges (rising or falling). It has two primary inputs:

1. **D (Data)** - Input signal to be stored.
2. **CLK (Clock)** - Synchronizes the operation.



D flip flop function is similar to that D latch, it stores data present in the data pin to the output pin only when the clock pin goes from low(0) to high (1) [in this design]

iii)1 bit register:

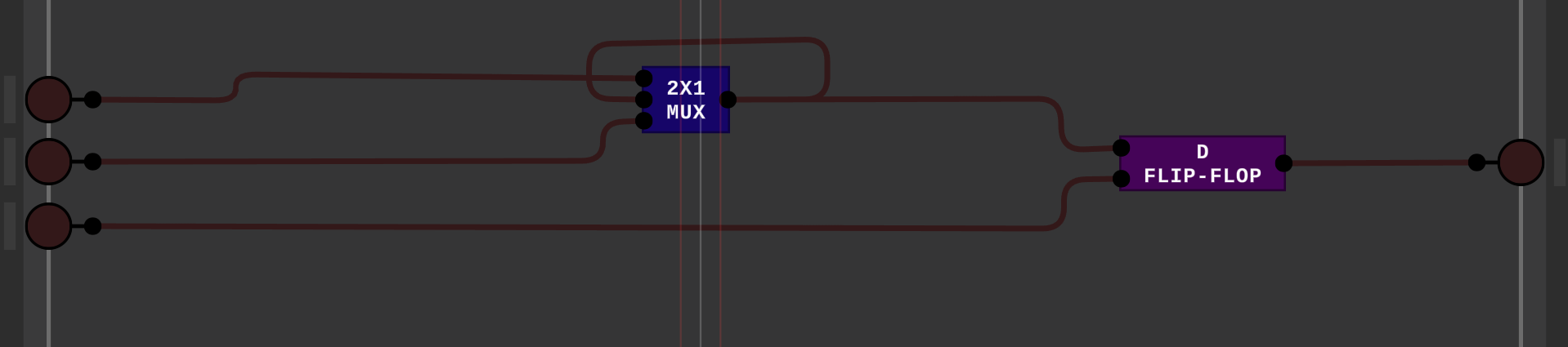
A **1-bit register** is a storage device capable of holding a single bit of data, either 0 or 1. It is built using a **D flip-flop** and includes control signals for operations like storing or updating the bit

It has 3 input pins

1)data pin

2)store pin

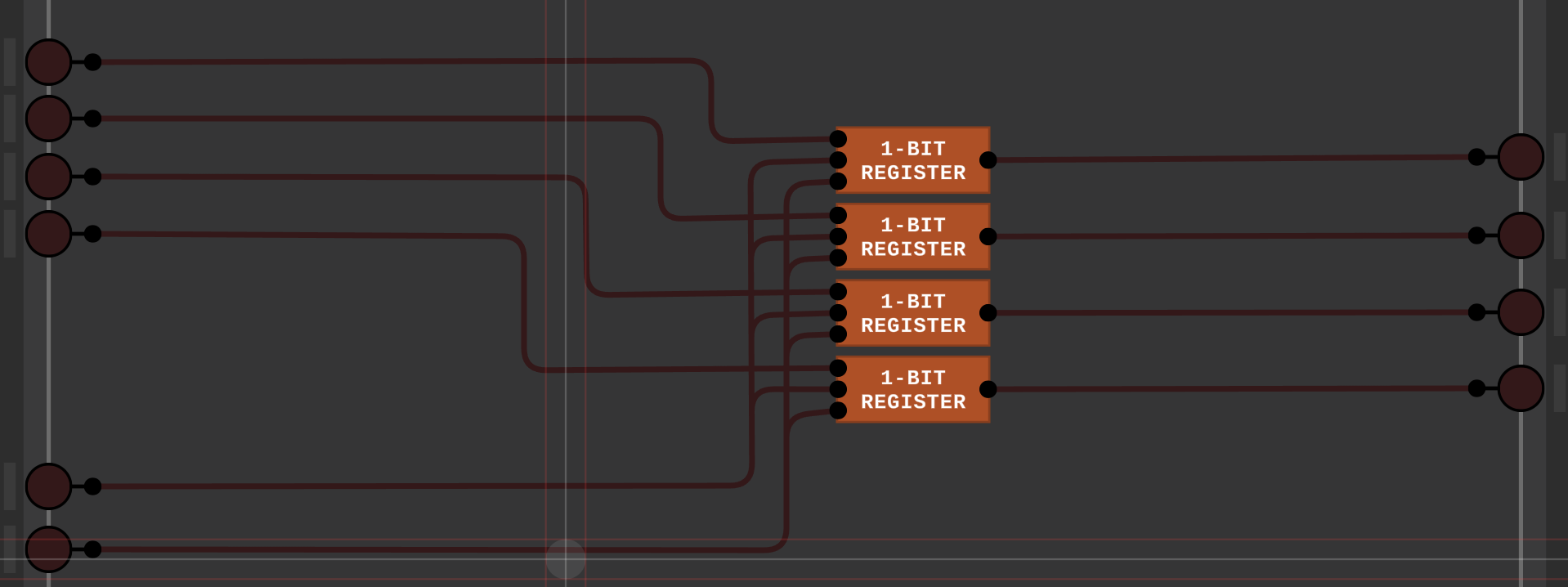
3)clock pin



The store pin decides whether the new data present in the data pin have to be stored in the output pin or not, for every spick in the clock pin (i.e. from low(0) to high(1))only this above operation will get a chance to perform.

iv)4 bit register:

This performs the same operation as of single bit register but instead of storing 1 bit this will store 4-bit



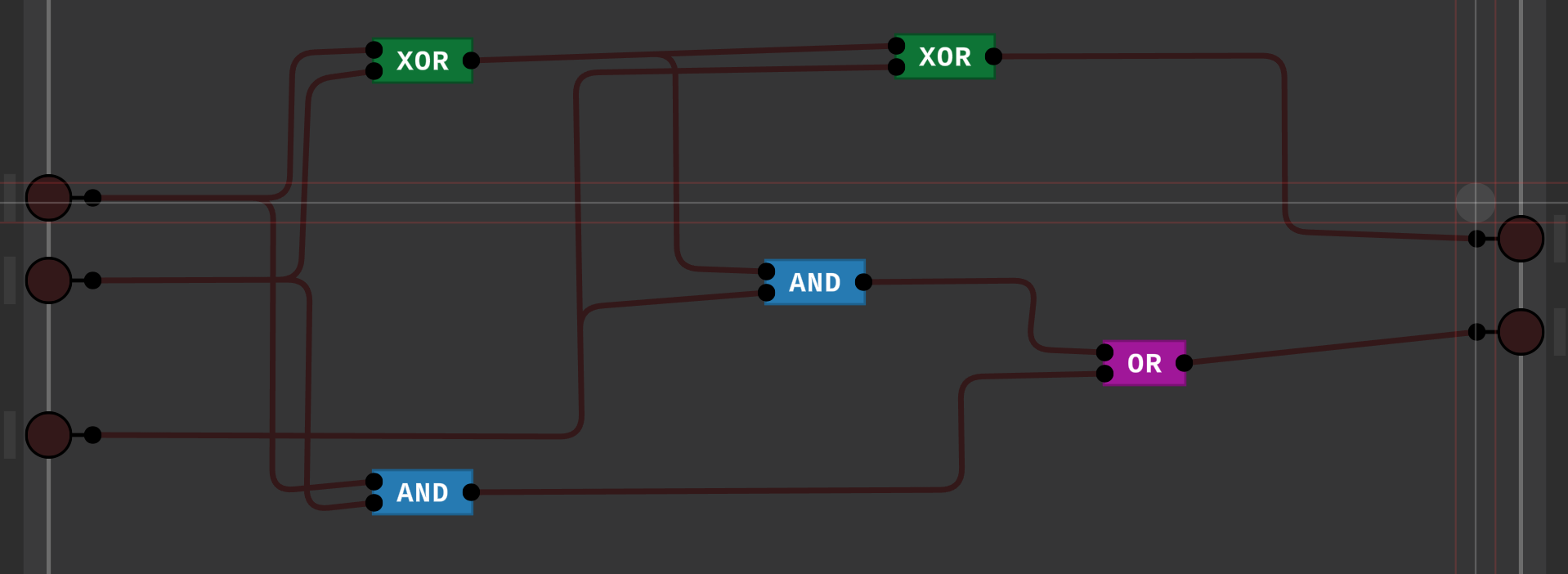
II)Arithmetic Logic Unit (ALU)[**EXPLAINED IN TASK 1**]

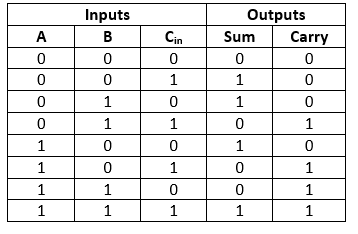
The Arithmetic Logic Unit (ALU) performs addition and subtraction as basic arithmetic operations. The ALU uses a sequence of logic gates to perform these operations.

i)ADDITION

a)ADDER:

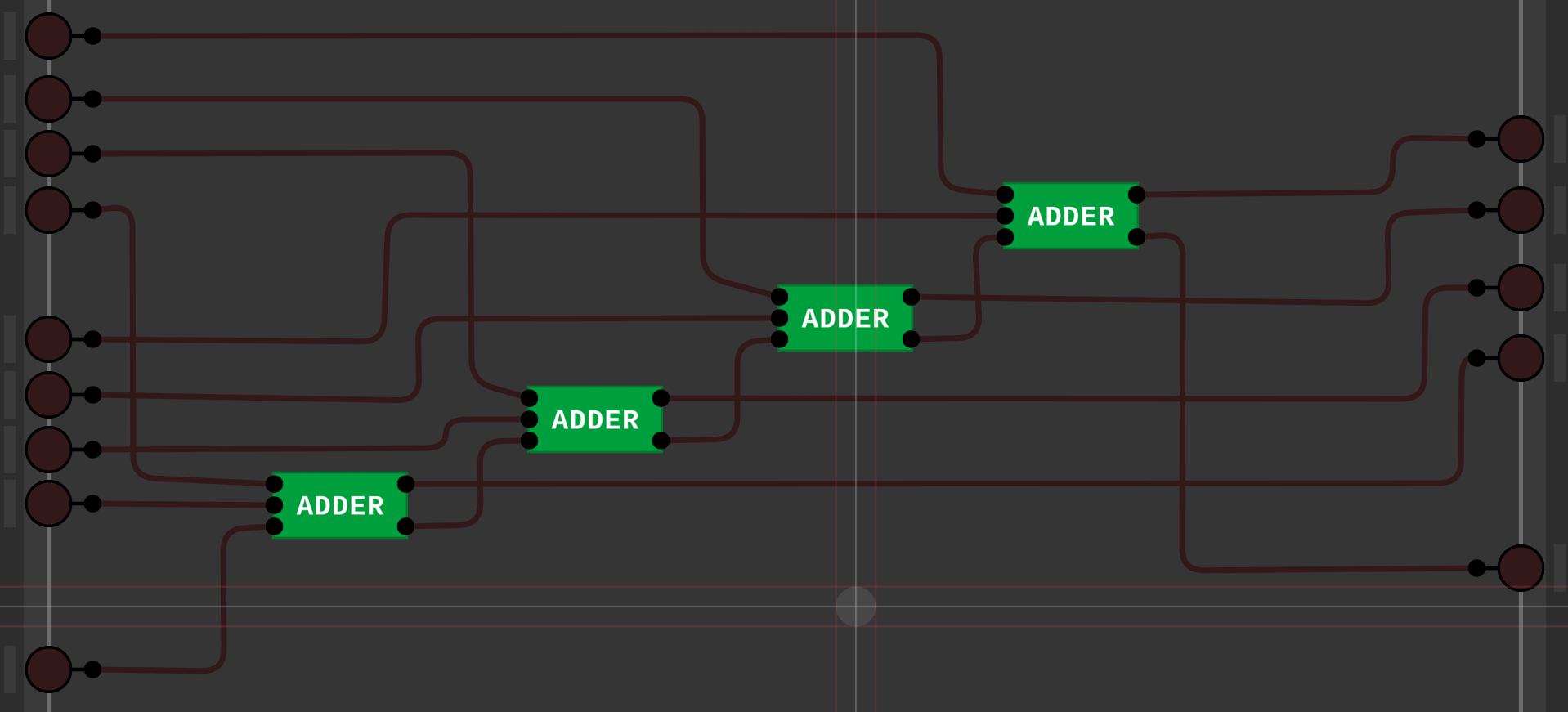
The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM. The C-OUT is also known as the majority 1’s detector, whose output goes high when more than one input is high.





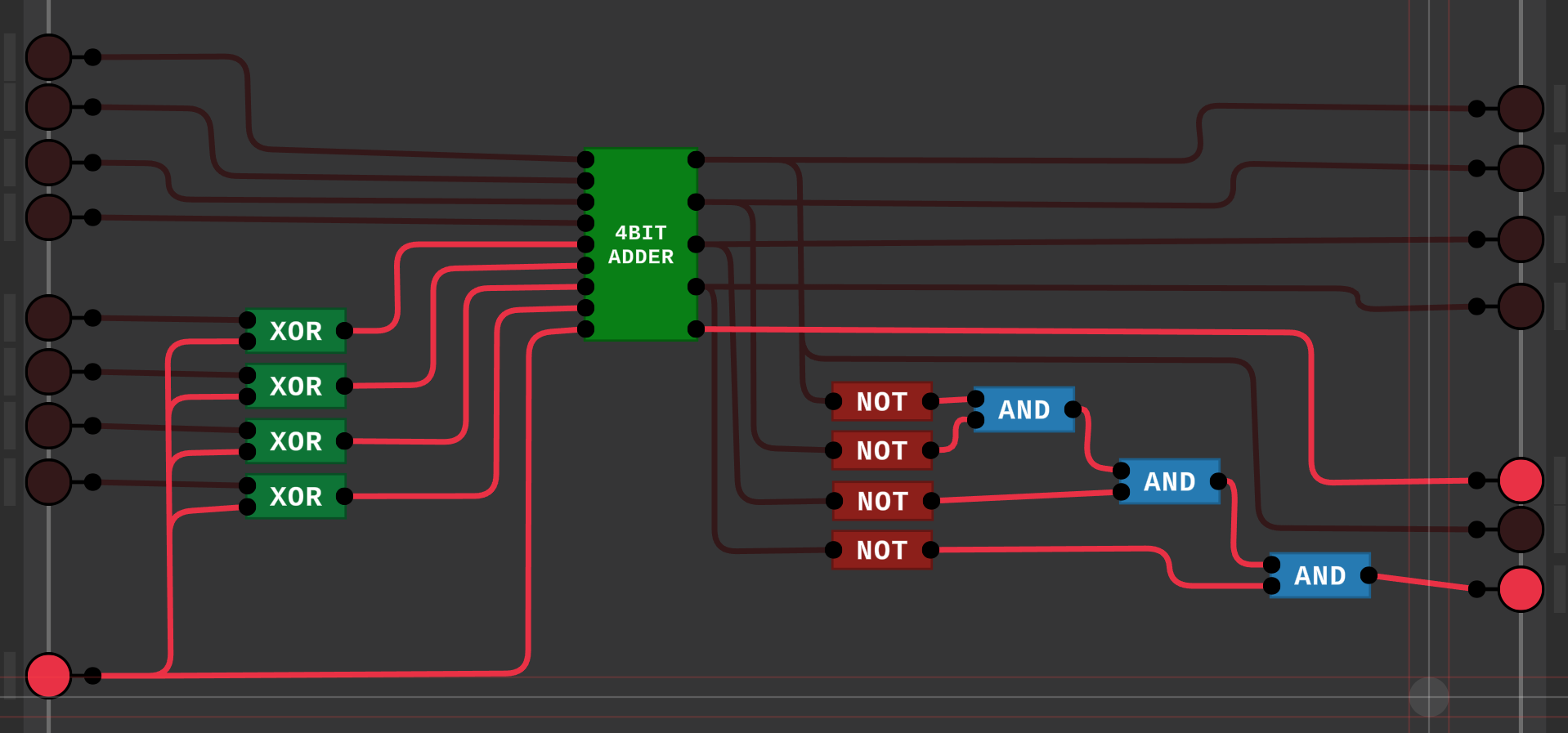
b)4BIT ADDER:

A full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to another.



ii)SUBTRACTION:

To subtract B from A, we must invert B and add 1 (2’s compliment). We convert B to -B and then we add -B to A to perform the subtraction operation

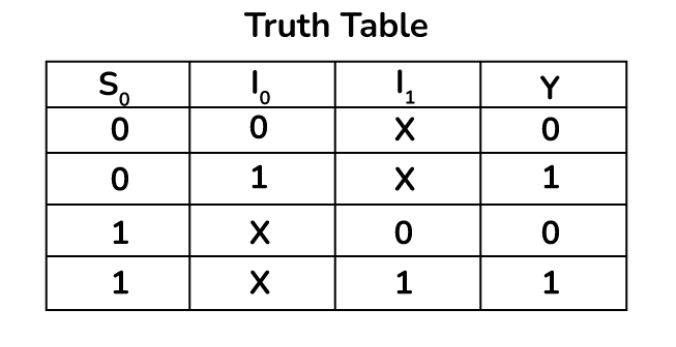


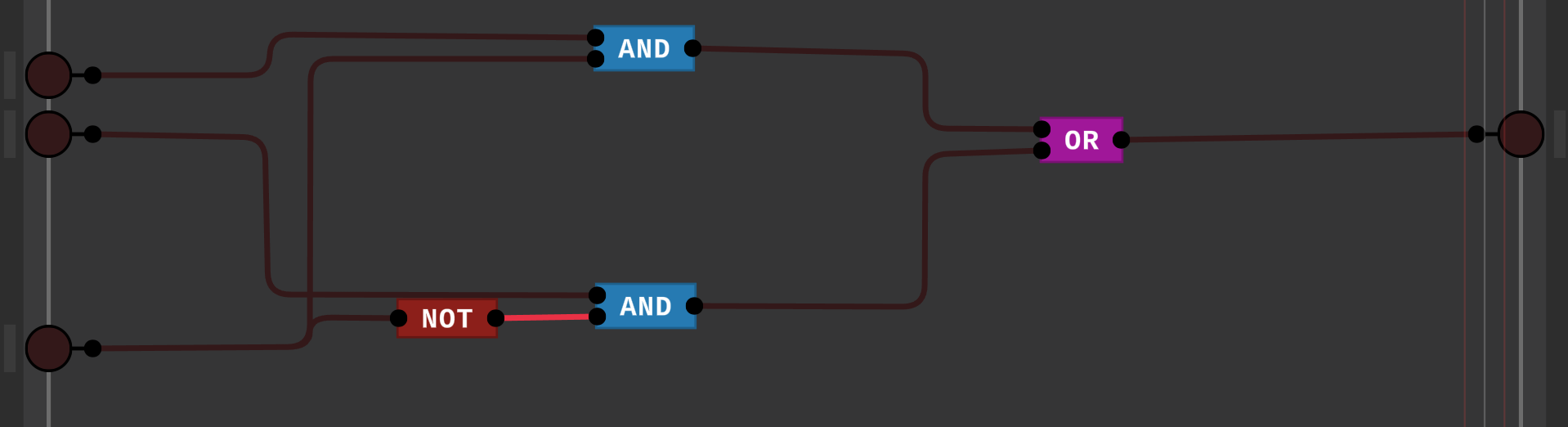
The working video has been uploaded in task 1.

III)Rest to 0

i)2x1 multiplexer:

it gets 2 inputs and based on the selector pin it decides which input has to be given as an output





ii)Rest to 0

total 4 such 2x1 multiplexers are in such way that it takes up 4 bit and it can either deliver that 4 bit or it can reset that 4 bit to 0 based on the selector pin

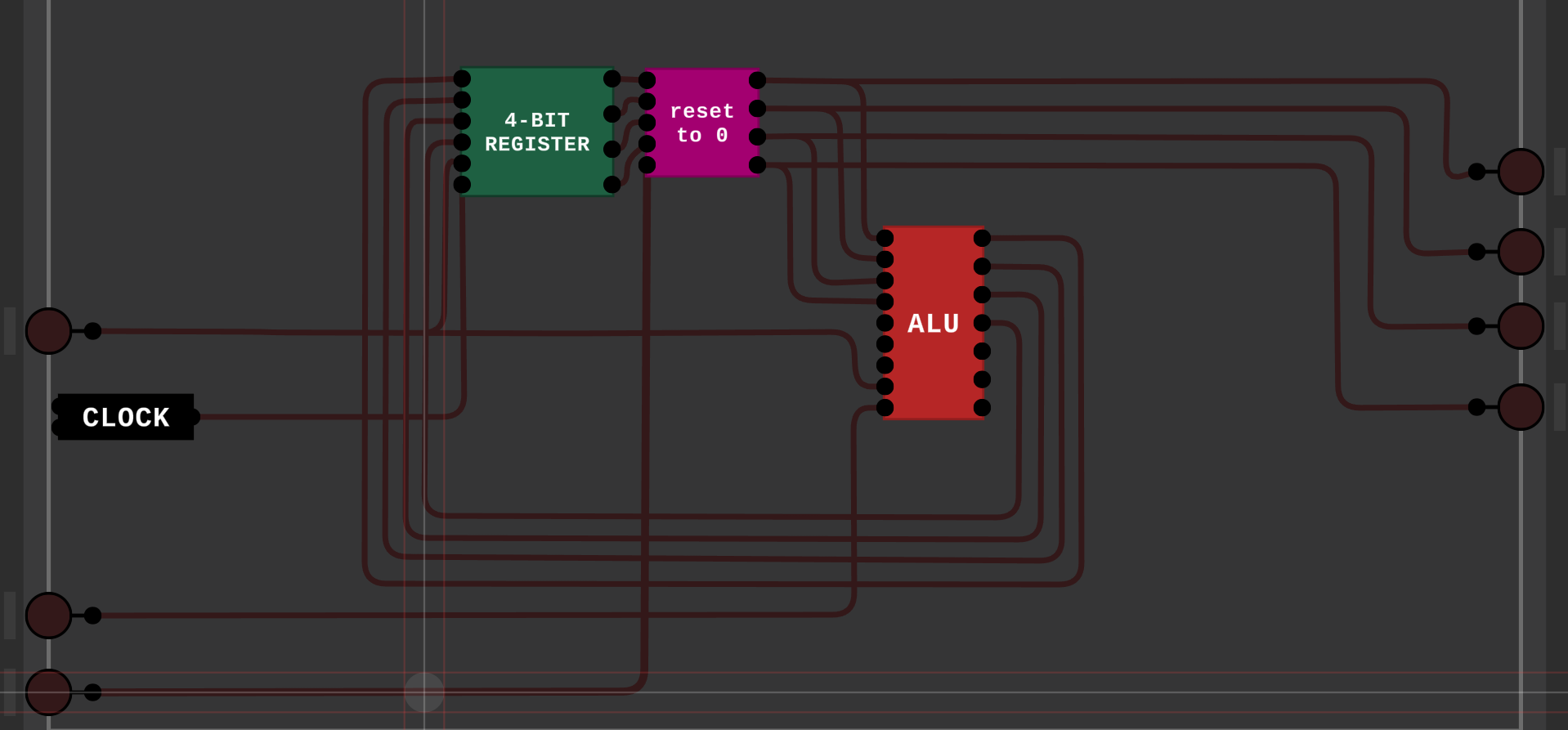


RESULT: 4-Bit Binary Counter

All the above 3 components (4-bit register, ALU and reset to 0) are arranged properly and it creates up 4-bit binary counter.

The clock will be on and off for every 1 second.

We have the start pin to start the operation, the up/down pin to count in forward and backwards directions and the reset pin to reset the count to 0



A working video of all the components are attached.